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conferences and other high-quality conferences in the broad-ranging fields of optics and photonics. These books provide prompt access to the latest innovations in research and technology in their respective fields. Proceedings of SPIE are among the most cited references in patent literature.

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ebooks for convenient reading. It is cross platform, running on Linux, Windows and OS X.

This book constitutes the refereed proceedings of the 23st International Symposium on VLSI Design and Test, VDAT 2019, held in Indore, India, in July 2019. The 63 full papers were

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carefully reviewed and selected from 199 submissions. The papers are organized in topical sections named: analog and mixed signal design; computing architecture and security; hardware design and optimization; low power VLSI and memory design; device modelling; and hardware implementation.

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This book describes in detail all required technologies and methodologies needed to create a comprehensive, functional design verification strategy and environment to tackle the toughest job of guaranteeing first-pass working silicon. The author first outlines all of the verification sub-fields at a high level, with just

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enough depth to allow an engineer to grasp the field before delving into its detail. He then describes in detail industry standard technologies such as UVM (Universal Verification Methodology), SVA (SystemVerilog Assertions), SFC (SystemVerilog Functional Coverage), CDV (Coverage Driven

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Verification), Low Power  
Verification (Unified  
Power Format UPF),  
AMS (Analog Mixed  
Signal) verification,  
Virtual Platform  
TLM2.0/ESL (Electronic  
System Level)  
methodology, Static  
Formal Verification,  
Logic Equivalency Check  
(LEC), Hardware  
Acceleration, Hardware  
Emulation,

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Hardware/Software Co-verification, Power Performance Area (PPA) analysis on a virtual platform, Reuse Methodology from Algorithm/ESL to RTL, and other overall methodologies.

This book explains integrated circuit design for manufacturability (DfM) at the product

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level (packaging, applications) and applies engineering DfM principles to the latest standards of product development at 22 nm technology nodes. It is a valuable guide for layout designers, packaging engineers and quality engineers, covering DfM development from 1D to 4D, involving IC design flow setup, best practices,

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links to manufacturing and product definition, for process technologies down to 22 nm node, and product families including memories, logic, system-on-chip and system-in-package.

The theme for the 2019 conference is Novel Computing Architectures. Papers will include discussions on



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the advent of Artificial Intelligence and the promise of quantum computing that are driving disruptive computing architectures; Neuromorphic chip designs on one hand, and Quantum Bits on the other, still in R&D, will introduce new computing circuitry and memory elements, novel materials, and different

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test methodologies.

These novel computing architectures will require further innovation which is best achieved through a collaborative Failure Analysis community composed of chip manufacturers, tool vendors, and universities.

For Electrical  
Engineering courses in  
analog layout or

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Manual professional layout designers. This text covers the issues involved in successfully laying out analog integrated circuits. Hastings provides clear guidance and does not stress theoretical physics or mathematical analysis of layouts. He emphasizes cross-sections of devices and carrier-based models of device operation as

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Manual  
compared to the more  
common geometric and  
schematic representation  
of devices.

A Wall Street Journal  
bestseller Owen  
Kiskaddon first came to  
the court of the  
formidable King Severn  
as a prisoner, winning  
favor with the stormy  
monarch by  
masquerading as a boy

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truly blessed by the Fountain. Nine years hence, the once-fearful Owen has grown into a confident young man, mentored in battle and politics by Duke Horwath and deeply in love with his childhood friend, the duke's granddaughter. But the blissful future Owen and Elysabeth Mortimer anticipate seems doomed

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by the king's  
machinations. A  
pretender to Severn's  
throne has vowed to seize  
the crown of  
Kingfountain. But Severn  
means to combat the  
threat by using Elysa<sup>b</sup>eth  
as bait to snare the  
imposter--and forcing  
Owen, as a pawn in the  
dangerous charade, to  
choose between duty and  
devotion. With poisoners

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and spies circling ominously, and war looming on the horizon, Owen must make painful sacrifices to beat back the advancing shadows of death and disaster. Will Owen's conflicted heart follow the king's path or will he risk everything for love?

This book constitutes the refereed proceedings of

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the 22st International  
Symposium on VLSI  
Design and Test, VDAT  
2018, held in Madurai,  
India, in June 2018. The  
39 full papers and 11  
short papers presented  
together with 8 poster  
papers were carefully  
reviewed and selected  
from 231 submissions.  
The papers are organized  
in topical sections  
named: digital design;



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analog and mixed signal design; hardware security; micro bio-fluidics; VLSI testing; analog circuits and devices; network-on-chip; memory; quantum computing and NoC; sensors and interfaces.

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